IN THE CLAIMS:

Kindly amend the claims, as follows:

1. - 47. (Canceled)

48. (Previously Presented) A pre-compensation circuit for recording of data signals, comprising:

a clock delay generator to generate clock delay data relative to a clock signal at a predetermined clock rate for each successive data signal to be recorded responsive to a pattern of adjacent data signals;

n clock delay units to control recording times of the successive data signals, wherein n >= 1,

wherein each of the clock delay units operates to generate an output signal for determining the recording time of one data signal in each sequence of n successive data signals responsive to the clock delay data received by the clock delay unit for the one data signal in the sequence;

a reference clock delay unit responsive to the clock signal for producing reference clock delay information at the predetermined clock rate; and

a calibrator responsive to the reference clock delay information for calibrating each of the n clock delay units to a change in the predetermined clock rate.

49. (Previously Presented) The pre-compensation circuit of claim 48, wherein a clock delay unit receives the clock delay data corresponding to a mth data signal of successive data signals in a clock period during which the clock delay unit that received the clock delay data corresponding to a (m-n+1)th data signal of the successive data signals generates the output signal for determining the recording time of a (m-n+1)th data signal.

50. (Previously Presented) The pre-compensation circuit of claim 48, wherein each clock delay unit comprises a reprogrammable clock delay unit that is reprogrammed for

the one data signal received in each sequence of successive data signals.

51. (Previously Presented) The pre-compensation circuit of claim 48, wherein each pattern of adjacent data signals includes at least one of a pattern of data signals immediately preceding the data signal for which the clock delay data is generated and a set of data signals immediately succeeding the data signal for which the clock delay data is generated.

52. (Previously Presented) The pre-compensation circuit of claim 48, wherein each pattern of adjacent data signals includes a pattern of data signals surrounding the data signal for which the clock delay data is generated.

53. (Previously Presented) The pre-compensation circuit of claim 48, further comprising:

a selector to select the output signals of the n clock delay units successively in each n data signal sequence to control the recording times of the successive data signals of the sequence so that the clock delay data for a mth data signal is received by one of the n clock delay units while the output signal of the clock delay unit that is to receive a (m+1)th data signal controls the recording time of a (m-n+1)th data signal.

54. (Previously Presented) The pre-compensation circuit of claim 48, wherein the clock delay generator comprises:

a look up table responsive to the pattern of adjacent data signals for forming clock delay data relative to the generated clock signal for each successive data signal.

55. (Previously Presented) The pre-compensation circuit of claim 48, wherein the clock delay generator comprises:

a look up table responsive to the pattern of adjacent data signals for each data signal to form clock delay information; and

a combining unit to combine the reference clock delay information with the look up

table formed clock delay information to generate the clock delay data for the data signal.

56. (Previously Presented) The pre-compensation circuit of claim 48, wherein the reference clock delay unit comprises:

a reprogrammable reference clock delay unit that is reprogrammed responsive to a change in the predetermined clock rate.

57. (Previously Presented) The pre-compensation circuit of claim 48, wherein the calibrator comprises:

a comparator for comparing the reference clock delay information to the output signals of the at least one clock delay unit to form an offset value for each clock delay unit.

58. (Previously Presented) The pre-compensation circuit of claim 48, wherein each clock delay unit includes an interpolator for interpolating the clock delay data.

59. (Previously Presented) The pre-compensation circuit of claim 48, wherein the at least one clock delay unit sequentially controls recording times of the successive data signals.

60. (Previously Presented) A method of pre-compensating recording of data signals, comprising the steps of:

generating clock delay data relative to a clock signal at a predetermined clock rate for each successive data signal to be recorded responsive to a pattern of adjacent data signals;

sequentially controlling recording times of the successive data signals by n clock delay units, wherein n >= 1,

wherein each of the clock delay units generates an output signal for determining the recording time of one data signal in each sequence of n successive data signals responsive to the clock delay data received by the clock delay unit for the one data signal of the sequence;

producing reference clock delay information at the predetermined clock rate

responsive to the clock signal; and

calibrating each of the n clock delay units to a change in the predetermined clock rate responsive to the reference clock delay information.

61. (Previously Presented) The method of claim 60, wherein a clock delay unit receives the clock delay data corresponding to a mth data signal of successive data signals in a clock period during which the clock delay unit that received the clock delay data corresponding to a (m-n+1)th data signal of the successive data signals generates the output signal for determining the recording time of the (m-n+1)th data signal.

62. (Previously Presented) The method of claim 60, wherein each clock delay unit is reprogrammed for the one data signal received in each sequence of n successive data signals.

63. (Previously Presented) The method of claim 60, wherein each pattern of adjacent data signals includes at least one of a pattern of data signals immediately preceding the data signal for which the clock delay data is generated and a set of data signals immediately succeeding the data signal for which the clock delay data is generated.

64. (Previously Presented) The method of claim 60, wherein each pattern of adjacent data signals includes a pattern of data signals surrounding the data signal for which the clock delay data is generated.

65. (Previously Presented) The method of claim 60, further comprising the step of:

selecting the output signals of the n clock delay units successively in each n data signal sequence to control the recording times of the successive data signals of the sequence so that the clock delay data for a mth data signal is received by one of the n clock delay units while the output signal of the clock delay unit that is to receive a (m+1)th data signal controls the recording time of a (m-n+1)th data signal.

66. (Previously Presented) The method of claim 60, wherein the step of generating the clock delay data comprises the step of:

obtaining clock delay information from a look up table responsive to the pattern of adjacent data signals for forming clock delay data relative to the generated clock signal for each successive data signal.

67. (Previously Presented) The method of claim 60, wherein the step of generating the clock delay data includes the steps of:

obtaining clock delay information from a look up table responsive to the pattern of adjacent data signals for each data signal; and

combining the reference clock delay information with the look up table formed clock delay information to generate the clock delay data for the data signal.

68. (Previously Presented) The method of claim 60, wherein the reference clock delay information is re-calibrated responsive to the change in the predetermined clock rate.

69. (Previously Presented) The method of claim 60, wherein the step of calibrating comprises the step of:

comparing the reference clock delay information to the output signals of the at least one clock delay unit to form an offset value for each clock delay unit.

70. (Previously Presented) The method of claim 60, wherein each clock delay unit interpolates the received clock delay data.

71. (Previously Presented) A pre-compensation circuit for recording of data signals, comprising:

clock delay generating means for generating clock delay data relative to a clock signal at a predetermined clock rate for each successive data signal to be recorded responsive to a pattern of adjacent data signals;

n clock delay means for controlling recording times of the successive data signals, wherein n >= 1,

wherein each of the clock delay means operates to generate an output signal for determining the recording time of one data signal in each sequence of n successive data signals responsive to the clock delay data received by the clock delay means in the sequence for the one data signal;

a reference clock delay means responsive to the clock signal for producing reference clock delay information at the predetermined clock rate; and

a calibration means responsive to the reference clock delay information for calibrating each of the n clock delay means to a change in the predetermined clock rate.

72. (Previously Presented) The pre-compensation circuit of claim 71, wherein a clock delay means receives the clock delay data corresponding to a mth data signal of successive data signals in a clock period during which the clock delay means that received the clock delay data corresponding to a (m-n+1)th data signal of the successive data signals generates the output signal for determining the recording time of the (m-n+1)th data signal.

73. (Previously Presented) The pre-compensation circuit of claim 71, wherein each clock delay means comprises:

reprogrammable clock delay means that is reprogrammed for the one data signal received in each sequence of successive data signals.

74. (Previously Presented) The pre-compensation circuit of claim 71, wherein each pattern of adjacent data signals includes at least one of a pattern of data signals immediately preceding the data signal for which the clock delay data is generated and a set of data signals immediately succeeding the data signal for which the clock delay data is generated.

75. (Previously Presented) The pre-compensation circuit of claim 71, wherein each pattern of adjacent data signals includes a pattern of data signals surrounding the data

signal for which the clock delay data is generated.

76. (Previously Presented) The pre-compensation circuit of claim 71, further comprising:

a selecting means for selecting the output signals of the n clock delay means successively in each n data signal sequence to control the recording times of the successive data signals of the sequence so that the clock delay data for a mth data signal is received by one of the n clock delay means while the output signal of the clock delay means that is to receive a (m+1)th data signal controls the recording time of a (m-n+1)th data signal.

77. (Previously Presented) The pre-compensation circuit of claim 71, wherein the clock delay generating means comprises:

means responsive to the pattern of adjacent data signals for looking up clock delay data relative to the generated clock signal for each successive data signal.

78. (Previously Presented) The pre-compensation circuit of claim 71, wherein the clock delay generating means comprises:

look up means responsive to the pattern of adjacent data signals for each data signal for forming clock delay information; and

combining means for combining the reference clock delay information with the look up means formed clock delay information to generate the clock delay data for the data signal.

79. (Previously Presented) The pre-compensation circuit of claim 71, wherein the reference clock delay means comprises:

a reprogrammable reference clock delay means that is reprogrammed responsive to a change in the predetermined clock rate.

80. (Previously Presented) The pre-compensation circuit of claim 71, wherein the calibration means comprises:

a comparing means for comparing the reference clock delay information to the output

signals of the at least one clock delay means to form an offset value for each clock delay means.

81. (Previously Presented) The pre-compensation circuit of claim 71, wherein each clock delay means includes:

interpolating means for interpolating the received clock delay data.

82. (Previously Presented) The pre-compensation circuit of claim 71, wherein the at least one clock delay means sequentially controls recording times of the successive data signals.

83. (Previously Presented) In a pre-compensation circuit for recording of data signals, a computer usable medium having computer readable program units embodied therein comprising:

a first program unit for determining clock delay data relative to a clock signal at a predetermined clock rate for each successive data signal to be recorded responsive to a pattern of adjacent data signals;

a second program unit for controlling sequential operation of n programmable clock delay units to determine the recording time of the successive data signals, wherein n >= 1,

wherein each of the programmable clock delay units is controlled to generate an output signal for determining the recording time of one data signal in each sequence of n successive data signals responsive to the clock delay data received by the programmable clock delay unit for the one data signal in the sequence;

a third program unit for producing reference clock delay information at the predetermined clock rate; and

a fourth program unit for calibrating each of the n programmable clock delay units to a change in the predetermined clock rate.

84. (Previously Presented) The computer usable medium of claim 83, wherein the second program unit controls a programmable clock delay unit to receive the clock delay data

corresponding to a mth data signal of successive data signals in a clock period during which the programmable clock delay unit that received the clock delay data corresponding to a (m-n+1)th data signal of the successive data signals generates the output signal for determining the recording time of the (m-n+1)th data signal.

85. (Previously Presented) The computer usable medium of claim 83, wherein the second program unit includes a program unit that reprograms each programmable clock delay unit for the one data signal received in each sequence of successive data signals.

86. (Previously Presented) The computer usable medium of claim 83, further comprising:

a fifth program unit for selecting output signals of the n programmable clock delay units successively in each n data signal sequence to control the recording times of the successive data signals of the sequence so that the clock delay data for a mth data signal is received by one of the n programmable clock delay units while the output signal of the programmable clock delay unit that is to receive a (m+1)th data signal controls the recording time of a (m-n+1)th data signal.

87. (Previously Presented) The computer usable medium of claim 83, wherein the first program unit includes:

a program unit for obtaining clock delay information from a look up table for each data signal responsive to the pattern of adjacent data signals; and

a program unit for combining the look up table clock data information for each data signal with the reference clock data information for the programmable clock delay unit to which clock delay data for the data signal is sent to form the clock delay data for the data signal.

88. (Previously Presented) The computer usable medium of claim 83, further comprising:

a fifth program unit responsive to a change in write clock rate for reprogramming the

reference clock delay information of each programmable clock delay unit responsive to the change in the predetermined clock rate.

89. (New) The pre-compensation circuit of claim 48, wherein $n > 1$.

90. (New) The method of claim 60, wherein $n > 1$.

91. (New) The pre-compensation circuit of claim 71, wherein $n > 1$.

92. (New) The computer usable medium of claim 83, wherein $n > 1$.